ABSTRACT OF THE DISCLOSURE

A system and method for initializing and resetting a clocking subsystem having a phased locked loop (PLL) within an input/output interface of a data processing system. A first timer generates signals in response to receiving clock signals from a clock source. A second timer detects the presence or absence of signals from the first timer and in response to an absence outputs a circuit reset signal to a circuit. The circuit in turn issues a reset signal to the PLL and to other systems